REMARKS

This application has been further reviewed in light of the Office Action dated March 23, 2006. Claims 1 to 12 and 14 to 16 remain pending in the application with Claim 13 having been canceled. Claims 1, 5, 6, 10, 14 and 15 are the independent claims herein. Reconsideration and further examination are respectfully requested.

Claims 15 and 16 were rejected under 35 U.S.C. § 102(b) over U.S. Patent No. 5,831,683 (Matsumoto), Claims 1, 2, 4, 6, 7 and 11 to 14 were rejected under 35 U.S.C. § 103(a) over U.S. Patent No. 5,961,616 (Wakasugi) in view of U.S. Patent No. 6,453,272 (Slechta), Claims 3, 5, 8 and 10 were rejected under § 103(a) over Wakasugi in view of Slechta and further in view of U.S. Patent No. 6,570,666 (Sotokawa), and Claim 9 was rejected under § 103(a) over Wakasugi in view of Slechta and further in view of U.S. Patent No. 6,175,603 (Chapman). Reconsideration and withdrawal of the rejections are respectfully requested.

The present invention relates to an interface apparatus (e.g., in a printer) fetching and outputting information input from an external apparatus. According to the invention, when information is input from the external apparatus, and a change is detected in the input information, the input information is fetched from the external apparatus. Then, a determination is made whether or not a protocol of the fetched information matches a protocol of the input information. If so, the fetched information is output (printed), if not, the fetched information is not output.

Referring specifically to the claims, amended independent Claim 1 is directed to an interface apparatus for inputting information from an external apparatus, comprising a first circuit for, in a case where there is a change in information input from the external apparatus, fetching the information after an elapse of a predetermined time,

and a second circuit for determining whether the information fetched by the first circuit matches a protocol of the information input from the external apparatus, and when the information fetched by the first circuit is matched with the protocol of the information input from the external apparatus, outputting the fetched information, and wherein, when the information fetched by the first circuit is not matched with the protocol of the information input from the external apparatus, the second circuit does not output the fetched information.

Independent Claims 5, 6 and 10 are directed to a printer, a method, and a printing method, respectively, and substantially correspond to Claim 1.

Independent Claim 14 includes features along the lines of Claim 1, but is more specifically directed to an interface apparatus for inputting information from an external apparatus, comprising a change detector for detecting a change in information input from the external apparatus and outputting a reset upon the detection of the change, a timer for inputting the reset output by the change detector and outputting a trigger after an elapse of a predetermined time from the input of the reset, a latch for inputting the trigger output by the timer and fetching information input from the external apparatus upon the input of the trigger, and a logical filter for determining whether the information fetched by the latch matches a protocol of the information input from the external apparatus, and when the information fetched by the latch is matched with the protocol of the information input from the external apparatus, outputting the fetched information, and wherein, when the information fetched by the latch is not matched with the protocol of the information input from the external apparatus, the logical filter does not output the fetched information.

Independent Claim 15 also includes features along the lines of Claim 1, but is more specifically directed to an interface apparatus for inputting information from an

external apparatus, comprising a timer for timing a predetermined time, a comparator for making a comparison between a length of a low level state in input information input from the external apparatus within the predetermined time timed by the timer, and a length of a high level state in the input information within the predetermined time, and for outputting a low level signal if the comparison shows that the length of the low level state is longer than the length of the high level state, and outputting a high level signal if the comparison shows that the length of the high level state is longer than the length of the low level state, and a logical filter for determining whether information indicated by the signal output by the comparator matches a protocol of the information input from the external apparatus, and when the information indicated by the signal output by the comparator is matched with the protocol of the information input from the external apparatus, outputting the indicated information, and wherein, when the information indicated by the signal output by the comparator is not matched with the protocol of the information input from the external apparatus, the logical filter does not output the indicated information.

The applied, alone or in any permissible combination, is not seen to disclose or to suggest the features of the present invention. With regard to Claims 1, 5, 6 and 10, the applied art is not seen to disclose or to suggest at least the features of determining whether information fetched by a first circuit after a predetermined time has elapsed when there is a change in input information from an external apparatus matches a protocol of the information input from the external apparatus, and when the information fetched by the first circuit is matched with the protocol of the information input from the external apparatus, outputting the fetched information, and wherein, when the information fetched by the first circuit is not matched with the protocol of the information input from the external apparatus, the second circuit does not output the fetched information.

Similarly, with regard to Claim 14, the applied art is not seen to disclose or to suggest at least the feature of a logical filter determining whether information fetched by a latch upon input of a trigger matches a protocol of information input from an external apparatus, and when the information fetched by the latch is matched with the protocol of the information input from the external apparatus, outputting the fetched information, and wherein, when the information fetched by the latch is not matched with the protocol of the information input from the external apparatus, the logical filter does not output the fetched information.

Along the same lines, with regard to Claim 15, the applied art is not seen to disclose or to suggest at least the feature of a logical filter determining whether information indicated by a signal output by a comparator matches a protocol of information input from an external apparatus, and when the information indicated by the signal output by the comparator is matched with the protocol of the information input from the external apparatus, outputting the indicated information, and wherein, when the information indicated by the signal output by the comparator is not matched with the protocol of the information input from the external apparatus, the logical filter does not output the indicated information.

With regard to the § 102 rejection of Claim 15, Matsumoto is merely seen to disclose a device that generates a clock signal by utilizing a phase comparator and a noise suppression device. Matsumoto is not, however, seen to teach the feature of a logical filter determining whether information indicated by a signal output by a comparator matches a protocol of information input from an external apparatus, and when the information indicated by the signal output by the comparator is matched with the protocol of the information input from the external apparatus, outputting the indicated information, and

wherein, when the information indicated by the signal output by the comparator is not matched with the protocol of the information input from the external apparatus, the logical filter does not output the indicated information as claimed in Claim 15. Accordingly, Claim 15 is not believed to be anticipated by Matsumoto.

Turning to the other independent claims, the Office Action admits that Wakasugi fails to teach the claimed second circuit. However, the Office Action cites Slechta as allegedly making up for Wakasugi's deficiencies.

Slechta is merely seen to disclose a system that identifies spurious noise values in an input signal and replaces them with substitute values representative of the spurious-noise-free signal, when the signal deviation exceeds a predetermined threshold. The system passes the signal unchanged when the signal deviation does not exceed the threshold. Slechta is not, however, seen to teach the claimed second circuit which either outputs or does not output information fetched by the first circuit based on a determination of whether the protocol of the fetched information matches a protocol of the input information. Thus, the proposed combination of Wakasugi and Slechta is not seen to teach the features of Claims 1, 5, 6 and 10.

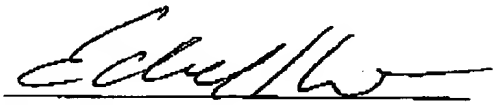
The other art of record, namely Sotokawa, and Chapman, are not seen to make up for the deficiencies of Wakasugi and Slechta, and any permissible combination of Wakasugi, Slechta, Sotokawa, and/or Chapman, is not believed to result in the above features of Claims 1, 5, 6, and 10.

In view of the foregoing deficiencies of the applied art, independent Claims 1, 5, 6, 10, 14 and 15, as well as the claims dependent therefrom, are believed to be in condition for allowance.

No other matters having been raised, the entire application is believed to be in condition for allowance and such action is respectfully requested at the Examiner's earliest convenience.

Applicants' undersigned attorney may be reached in our Costa Mesa, California office at (714) 540-8700. All correspondence should continue to be directed to our below-listed address.

Respectfully submitted,



Edward A. Kmett
Attorney for Applicants
Registration No.: 42,746

FITZPATRICK, CELLA, HARPER & SCINTO
30 Rockefeller Plaza
New York, New York 10112-3800
Facsimile: (212) 218-2200

CA_MAIN 114091v1